REMARKS

I. Introduction

Claims 1, 6-9, 17, 26, and 35 have been amended to more particularly define applicants' invention. Claims 2-5, 10-16, 18-25, 27-34, and 36-40 are also in the case.

Reconsideration of this application in light of the following remarks is respectfully requested.

II. The Claim Objections Based on Alleged Informalities

Claims 1, 6, 8, 9, 17, 26, and 35 have been objected to because of alleged informalities. All of these claims have been amended as suggested by the Examiner to cure these informalities.

III. The Rejections Based on 35 U.S.C. § 102

Claim 1 has been rejected under 35 U.S.C. § 102 as anticipated by Narasimhan et al. U.S. patent 6,446,192 ("the '192 patent"). This rejection is respectfully traversed.

Claim 1 relates to use of an integrated circuit chip that includes programmable logic circuitry. Claim 1 says that programmable logic circuitry on the chip is first used as the port through which a connection is made. Reprogramming data is brought into the chip via that port. Then that reprogramming data is used to reprogram the programmable logic circuitry to give that circuitry a function other than a communications port function. This is not shown in the '192 patent.

The Office action attempts to equate the "programmable input/output port" 82 in the '192 patent

with the programmable logic circuitry in applicants' claim 1. Circuitry 82 may be programmable, but there is no evidence that it has any other use than as input/output port circuitry. There is no evidence that circuitry 82 can be the port through which reprogramming data is brought into device 36, and that this reprogramming data can then be used to give circuitry 82 another function, in particular a function other than as a communications port. Again, there is no evidence that programmable input/output port 82 in the '192 patent is ever used or usable as anything other than input/output port (i.e., communications) circuitry.

Because the above-discussed feature of claim 1 is not shown in the '192 patent, claim 1 is not anticipated by the '192 patent. Claim 1 and its dependent claims 2-5 should accordingly be allowed.

Claim 6 has been rejected on the same basis as claim 1, namely, anticipation by the '192 patent. This rejection is also respectfully traversed.

Claim 6 has been amended to call for "operating the integrated circuit chip to break at least one of the first and second connections after that connection has been used in the transferring of data." The '192 patent does not say anything about using connections from device 36 to other devices 38 or 32 only temporarily to get programming data, and thereafter having the device 36 break one or both of those connections. Certainly the connection between devices 36 and 38 seems permanent, because device 36 exists to monitor the performance of device 38. There is also no mention in the '192 patent of device 36 itself operating to break a connection 32 after device

36 has received configuration information via connection 32. Claim 6 is therefore not anticipated by the '192 patent, and claim 6 and its dependent claim 7 should accordingly be allowed.

Claim 8 has been rejected on the same basis as claim 1, namely, anticipation by the '192 patent. This rejection is respectfully traversed.

Claim 8 specifies programming programmable logic circuitry to function as Ethernet MAC circuitry and to thereafter reprogram the programmable logic circuitry to function as something other than Ethernet MAC circuitry. The '192 patent may show programmable I/O 82, but it does not show using that I/O first as one type of I/O (e.g., as Ethernet MAC circuitry) and then reprogramming I/O 82 to function as something else. In other words, the '192 patent may show programming I/O 82, but it does not show reprogramming that circuitry to switch it from some initial function to another, different function. Claim 8 is therefore not anticipated by the '192 patent, and claim 8 should accordingly be allowed.

Claim 9 has been rejected on the same basis that claim 1 was rejected, namely, anticipation by the '192 patent. This rejection is respectfully traversed.

Claim 9 has been amended to specify that after establishing a connection to an external data source and bringing in data from that source, the Ethernet MAC circuitry is operative to sever that connection. Claim 9 has been further amended to make it clear that the data thus brought into the chip is used to program programmable logic circuitry for chip operation subsequent to severing the Ethernet MAC connection.

This subject matter of claim 9 is not shown in the '192 patent. The '192 says nothing about chip 36 severing a connection it has made to external components 38 or 32. Nor does the '192 patent say anything about continued operation of device 36 after it has severed such a connection. Device 36 in the '192 patent may respond to different clients 30 at different times, but it does not appear that device 36 has the capability to both initiate and then terminate a connection to an external device. Device 36 appears passive with respect to requests from different clients 30 for a connection to be made or broken.

The foregoing establishes that claim 9 is not anticipated by the '192 patent. Claim 9 and its dependent claims 10-16 should accordingly be allowed.

Claim 17 has been rejected on the same basis as claim 1, namely, anticipation by the '192 patent. This rejection is respectfully traversed.

Claim 17 specifies Ethernet MAC circuitry that is operative to establish a connection for bringing programming data into the chip and to thereafter sever that connection. As has been pointed out above in connection with other claims, the '192 patent does not teach that device 36 includes the capability of severing a connection to an external configuration data source. Claim 17 is therefore not anticipated by the '192 patent. Claim 17 and its dependent claims 18-25 should accordingly be allowed.

Claim 26 has been rejected on the same basis as claim 1, namely anticipation by the '192 patent. One again this rejection is respectfully traversed.

Claim 26 specifies that the integrated circuit includes the capability of making two different

connections and also severing both of those connections. The '192 patent does not describe device 36 as having the capability of severing connections to external components or devices. Accordingly, claim 26 is not anticipated by the '192 patent. Claim 26 and its dependent claims 27-34 should therefore be allowed.

Claim 35 has also been rejected as anticipated by the '192 patent. This rejection is again respectfully traversed.

Claim 35 specifies that the programmable logic circuitry is operative to establish a connection, and to thereafter sever that connection. Once again, this capability of severing a connection is not shown in the '192 patent. Claim 36 is therefore not anticipated by the '192 patent, so that claim 35 and its dependent claims 36-40 should be allowed.

IV. Conclusion

The foregoing demonstrates that claims 1-40 are allowable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,

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